What Is Claimed Is

~~Patent Claims~~

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1. A method for communication among equal-access stations (2,..., 12) of a ring-shaped, serial fiber-optic bus, one station, during one bus cycle, generating strictly time-cyclical container messages (CT), addressing them, and supplying them to the serial bus, this station (2) supplying to the bus, as the end message of each bus cycle, a synchronization message, each station (2,..., 12) writing its data in the container messages (CT) addressed to it, each station (2,..., 12), as a function of its read authorization, reading the data of the written-in container messages (CT) on the serial bus, each station (2,..., 12) generating from the synchronization message that has been read an interrupt, which, depending on the position of the stations (2,..., 12) on the serial bus, is time delayed such that all interrupts are output in a time-synchronous manner, and, when the interrupts are output, all the data that have been read in the stations (2,..., 12) are further processed.

2. The method as recited in Claim 1, the time delay of an interrupt of one station being calculated in accordance with the following equation

$$t_{vz.n} = [N - (n - 1)] \cdot 3B$$

where N = number of users
B = bit time
n = location number of the station.

3. The method as recited in Claim 1 or 2, addressed blank messages, following the last addressed container message (CT), being continually provided to the serial bus.

4. The method as recited in one of Claims 1 through 3, special messages for filling up the bus cycle being output between the last generated addressed blank message and the synchronization

message.

5. The method as recited in one of Claims 1 through 4, the addressing and the output of the continually produced container messages (CT) being carried out in accordance with the increasing (rising) address part.

6. The method as recited in one of Claims 1 through 5, the addressing and the output of the continually generated container messages (CT) being carried out in accordance with the increasing (rising) subaddress part.

7. A device for carrying out the method of communication among equal-access stations (2,..., 12) of a ring-shaped, serial fiber-optic bus as recited in Claim 1, each station (2,..., 12) having an interface module (18), which, in each case, is connected to the serial fiber-optic bus by two bus connector sockets (42, 44), one station (2) on the bus being parametrized as dispatcher and the other stations (4,..., 12) as transceivers, the dispatcher station (2) containing a list of all messages (CT) to be transmitted, and each transceiver station (4,..., 12) having a read authorization.

8. The device as recited in Claim 6, the interface module (18) having a programmable microchip (20) having an associated erasable read-only memory (22), a read-write memory (16), and a clock generator (24), the interface module having a system connector (26), an opto-electrical and electro-optical converter (28, 30), and a voltage source (32), each bus connector socket (42, 44) being linked to the programmable microchip (20) by the converter (28, 30), and this programmable microchip (20) being connected to the system connector (26) via signal lines.

9. The device as recited in Claim 7 or 8, the interface module (18) having a plurality of light-emitting diodes (36, 38, and 40) for status display.

10. The device as recited in one of Claims 7 through 9, a programmable gate array being provided as the programmable microchip (20).

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Add B3